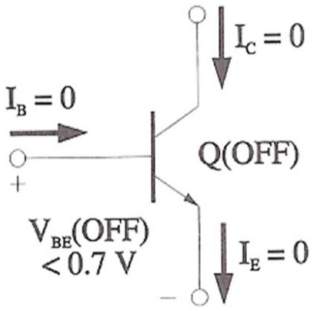
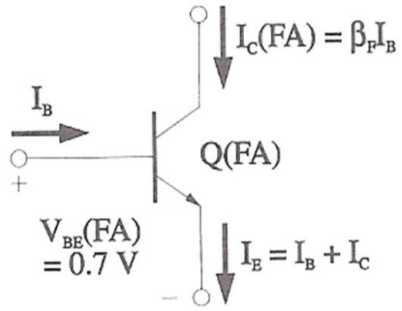
Introduction to Bipolar Digital Circuits

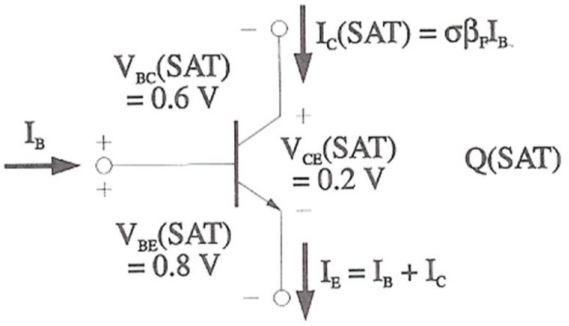
Analysis of BJT circuits with known states

BJT has four modes of operation
1. cutoff mode
2. forward active mode
3. saturation mode
4. reverse active mode

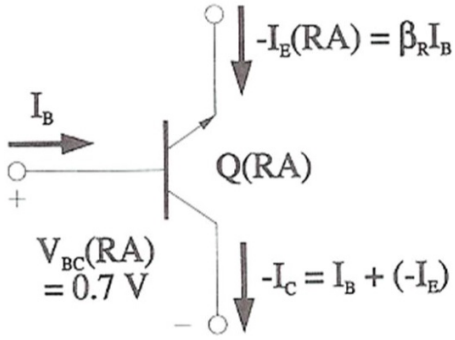
* The relationships for these modes are shown in the next figures:







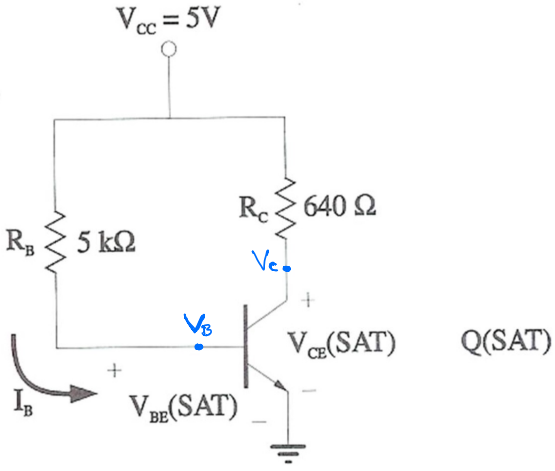
$(0 < \sigma < 1)$



* Usually $50 \leq \beta_F \leq 200$.

Example 4.1 ***BJT Saturation***

Determine the base and collector currents and σ for the saturated BJT in Figure 4.3. Let $\beta_F = 65$.



Since the BJT is in saturation mode & the emitter is at ground

$$V_B = V_{BE(sat)} = 0.8V$$

$$V_C = V_{CE(sat)} = 0.2V$$

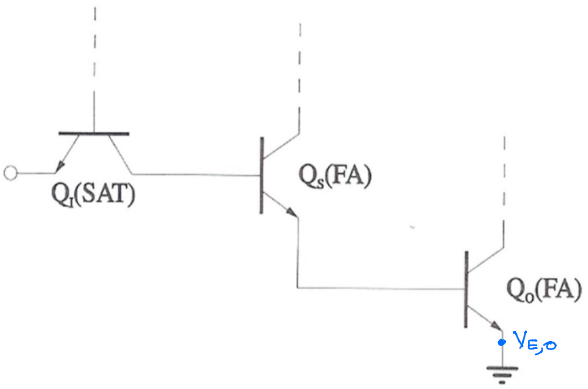
$$I_B = \frac{V_{CC} - V_{BE(sat)}}{R_B} = \frac{5 - 0.8}{5K} = 840\mu A$$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{5 - 0.2}{640} = 7.5\ mA$$

$$I_{C(sat)} = \sigma \beta_F I_B \Rightarrow \sigma = \frac{I_C}{\beta_F I_B} = \frac{7.5m}{65 \times 840\mu} = 0.137$$

Example 4.2 ***BJT Analysis with Known States***

Figure 4.4 shows a portion of a digital circuit where the state of each transistor is known. Solve for the voltages at the base and emitter of each BJT.



Q_O is FA

$V_{E,O} = 0V$

$V_{B,O} = V_{BE,O(FA)} = 0.7V$

Q_S is FA

$V_{E,S} = V_{B,O} = 0.7V$

$V_{B,S} = V_{BE,O}(FA) + V_{BE,S}(FA)$

$= 2V_{BE}(FA) = 2(0.7) = 1.4V$

Q_I is saturated

$V_{E,I} = V_{BE,O}(FA) + V_{BE,S} - V_{CE,I(sat)}$

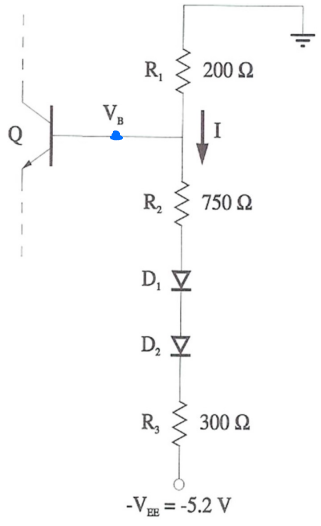
$= 2(0.7) - 0.2 = 1.2V$

$V_{B,I} = V_{E,I} + V_{BE,I}(sat)$

$= 1.2 + 0.8 = 2V$

Example 4.3 ***Diode Analysis with Known States***

Determine the current I through the branch in Figure 4.5. Also, find the voltage at the base of the transistor Q. Assume the BJT base current is negligible.



Using KVL

$GND - IR_1 - IR_2 - V_{D1(ON)} - V_{D2(ON)} - IR_3 + V_{EE} = 0$

$$I = \frac{V_{EE} - 2V_{D(ON)}}{R_1 + R_2 + R_3} = \frac{5.2 - 2(0.7)}{(200) + (750) + (300)} = 3.04\ mA$$

$V_B = GND - IR_1 = 0 - (3.04m)(200) = -608mV$

Notes:

For diode

$V_D(ON) = 0.7V$

For BJT

FA: $V_{BE} = 0.7V$ & $I_C = \beta_F I_B$

Sat: $V_{BE} = 0.8V$ & $V_{BC} = 0.6V$ & $V_{CE} = 0.2V$ &

$\sigma = \frac{I_C}{\beta_F I_B}$

RA: $V_{BC} = 0.7V$ $\quad I_E = \alpha_R I_C = -\beta_R I_C$

$\beta_R = \frac{\alpha_R}{1-\alpha_R}$, $\beta_R << \beta_F$ & $\beta_F = \frac{\alpha_F}{1-\alpha_F}$

For Schottky diode:

$V_{SBD}(ON) = 0.3V$

For Schottky clamped BJT:

F.A (SBD not conducting): $V_{BE}(ON) = 0.7V$

ON HARD: $V_{BE}(HARD) = 0.8V$

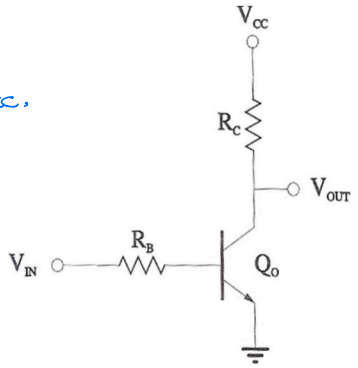
& $V_{BC}(ON) = V_{SBD}(ON) = 0.3V$

& $V_{CE}(HARD) = 0.5V$

* Schottky-clamped BJT is simply a BJT with schottky barrier diode connected between the base & collector. This diode prevents the BJT from operating in the saturation region.

BJT Inverter

* The circuit consists of a BJT with base & collector resistors & one voltage source V_{CC}.



* Output High Voltage $= V_{OH}$

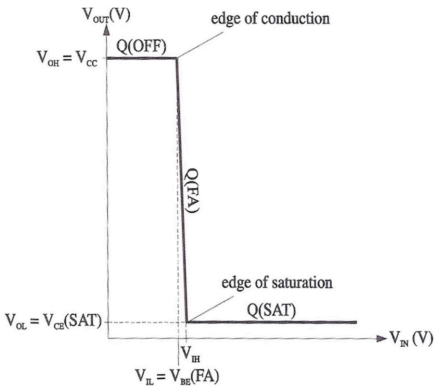
$\therefore V_{BE} < V_{BE}(FA)$

$\therefore$ BJT is cutoff

& $I_C = I_{RC} = 0$

$\Rightarrow$ There is no voltage drop across R_C

$$V_{out} = V_{CC} = V_{OH} \Rightarrow I_{C(OH)} = 0$$



* Input Loco Voltage $\equiv V_{IL}$

when $V_{BE} = V_{BE(FA)}$ the BJT is at the edge of conduction where the cutoff & forward active regions meet.

$$V_{IL} = V_{BE(FA)}$$

when V_{IN} passes $V_{BE(FA)}$ the voltage $V_{IN} - V_{BE(FA)}$ across R_B corresponds to $I_B = I_{RB}$
$I_C = \beta_F I_B$ & V_{out} decreses by $I_C R_C$

* Output Low Voltage $\equiv V_{OL}$

Increasing V_{in} to point of saturation

$$V_{OL} = V_{CE(sat)}$$

V_{CE} is the minimum collector-emitter voltage.

* Input High Voltage $\equiv V_{IH}$

V_{IH} is the input voltage at the edge of saturation & is also defined to be at the edge of the active region.

@ $V_{CE} = V_{CE(sat)}$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

@ edge of saturation $\sigma = 1 \Rightarrow I_C = \beta_F I_B$

$$I_{B(EOS)} = \frac{I_C}{\beta_F} = \frac{V_{CC} - V_{CE(sat)}}{\beta_F R_C}$$

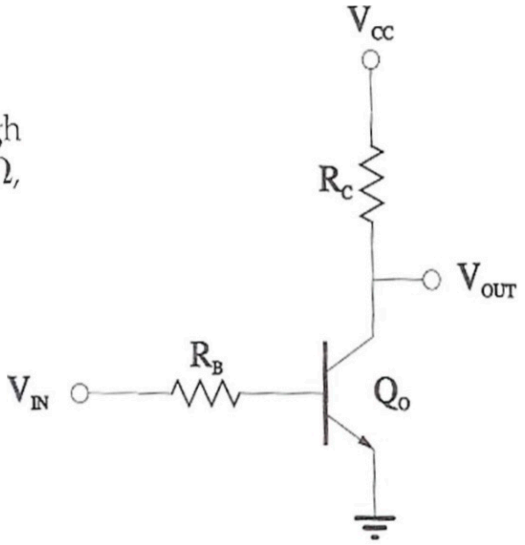
$\therefore V_{BE} = V_{BE(sat)}$

$$V_{IH} = V_{BE(sat)} + I_{B(EOS)} R_B$$

$$= V_{BE(sat)} + \left(\frac{V_{CC} - V_{CE(sat)}}{\beta_F R_C}\right) R_B$$

Example 4.4 ***BJT Inverter Voltage Transfer Characteristic***

For the BJT inverter of Figure 4.6, determine the high and low noise margins for $V_{CC} = 5$ V, $R_B = 10$ kΩ, $R_C = 1$ kΩ, and $\beta_F = 60$.



$V_{CC} = 5V \quad R_B = 10k\Omega \quad R_C = 1k\Omega$

$\beta_F = 60$

$V_{OH} = V_{CC} = 5V$

$V_{IL} = V_{BE(FA)} = 0.7V$

$V_{OL} = V_{CE(sat)} = 0.2V$

$$V_{IH} = V_{BE(sat)} + \left(\frac{V_{CC} - V_{CE(sat)}}{\beta_F R_C} \right) R_B$$

$$= 0.8 + \frac{(5 - 0.2)}{60 \times 1k} \times 10k = 1.6V$$

$V_{NMH} = V_{OH} - V_{IH} = 5 - 1.6 = 3.4V$

$V_{NML} = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5V$

* The low noise margin of the simple BJT inverter is unacceptably small.

TTL Super-Circuitry.

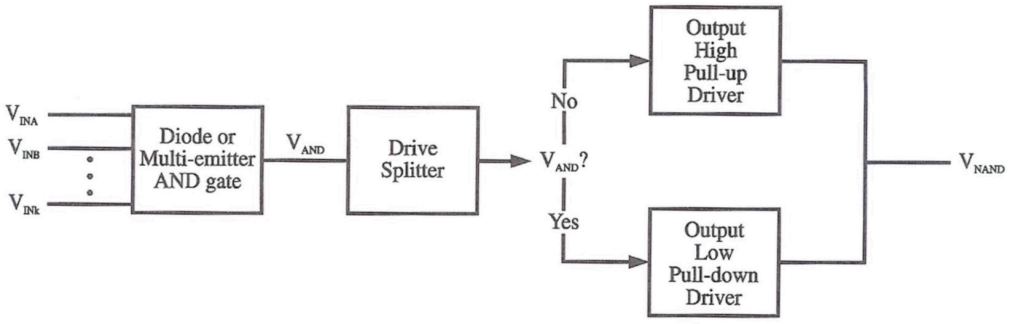


FIGURE 4.7 TTL Family Super-circuitry Block Diagram

Input Section:

the input section consists of an ANDing of all inputs

Drive Splitter

* the drive splitter turns on one of the two output sections
* A typical drive splitter is the BJT inverter we saw previously
* If the output of the AND gate is logic Low the input voltage to the drive splitter is also Low.
* For a logic high output from the AND gate the opposite output results
* the two output drivers are never on simultaneously.
* the drive splitter also provides additional base driving current to the output-low pull-down driver.
* while the input stage ANDs the multiple inputs the drive splitter section provides inversion
* if all inputs are connected together the logic circuit then reduces to an inverter

Output-High Pull-Up Drivers

* As the output goes low-to-high current is required to charge the equivalent capacitance of the load gates & the output-high pull-up section provides sourcing current for this charging
* It can be represented as

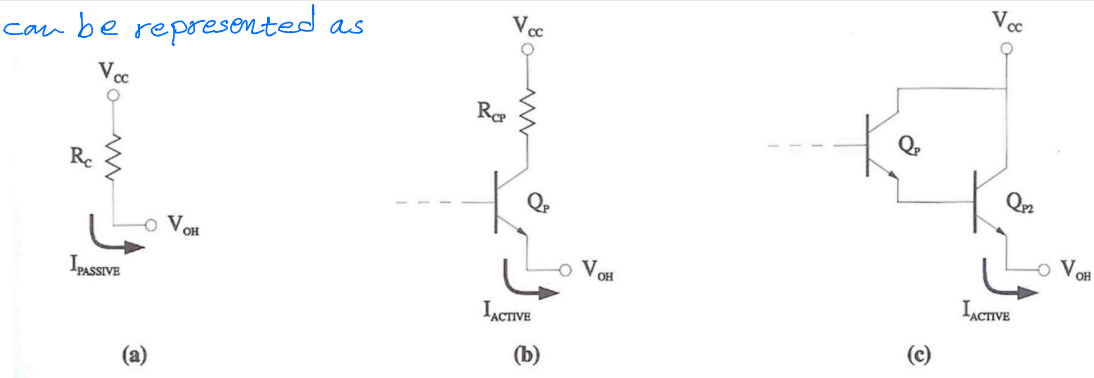


FIGURE 4.8 Pull-up Current Sources: (a) Passive, (b) Active, (c) Darlington pair active

(a) voltage driven resistor

(b) An emitter-follower which provides a higher sourcing current & therefore, faster switching time.

(c) Darlington pair configuration provides the highest sourcing current among these three & it is provides greater fan-out

Output-Low Pull-Down Driver

* Provides large sinking current to discharge the capacitive load
* Provides larger fan-out by sinking (non-zero) currents I_{IL} from all the load gates
* The current I_{OL} is collector current for a BJT and allows enough fan-out.

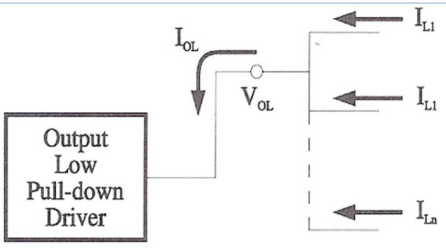


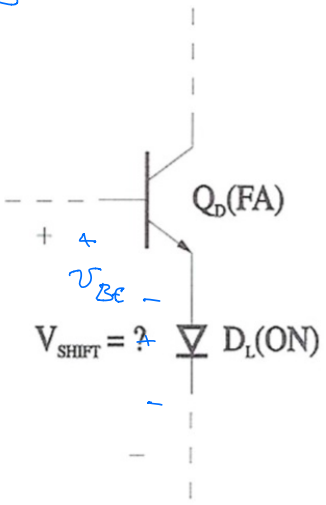
FIGURE 4.9 Fan-out Current Sinking

Level Shifting BJTs

The conducting diode voltage $V_{D(ON)} = 0.7V$ is an ideal element for level-shifting but alternatively the BE portion of a BJT can also be used for level-shifting and has the advantage of providing additional driving current.

Example 4.5 *Level-Shifting*

What is the level-shifting voltage V_{SHIFT} of the BJT-diode pair in Figure 4.10? Assume the BJT is forward-active and the diode is conducting.

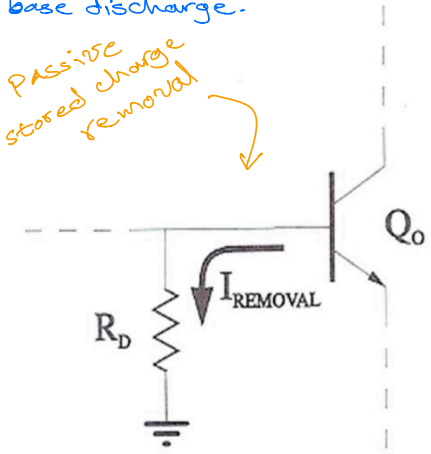


$$V_{shift} = V_{BE(FA)} + V_{D(ON)}$$
$$= 0.7 + 0.7 = 1.4\ V$$

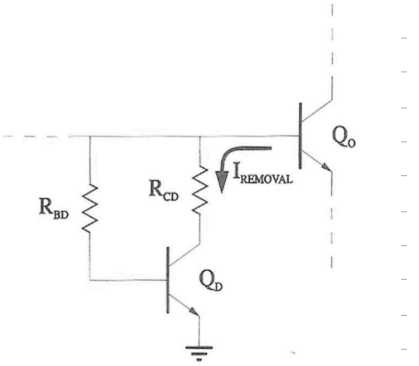
Discharge Paths & Base Driving Circuitry

* In order to turn off a saturated BJT, all of the stored charge in the base region must be removed. A path must therefore be available for base discharge.
* The resistor R_D provides passive charge removal
* The current magnitude is the base voltage of Q_O divided by the resistor:

$$I_{RD} = \frac{V_{BO}}{R_D}$$



* Active configuration for stored charge removal provides a much faster discharge than R_D.



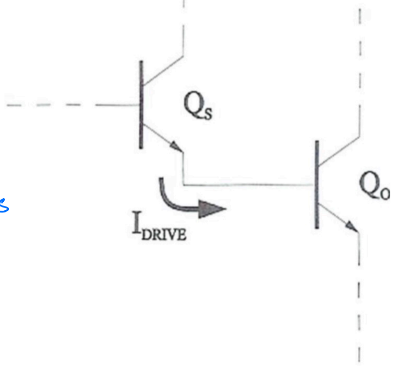
Active stored charge removal

* The turn on time of a BJT is dependent on the time required to charge the base of the BJT.

* Active base driving current is often supplied to BJTs that require a brief switching time.

* Emitter follower BJT configuration usually provides this driving current.

* the figure to the right shows an emitter-follower Q_S that provides base driving current to Q_o.



Self-Biasing BJTs

* If the resistors R_B & R_C of the self-biasing BJT are chosen properly the BJT will operate in the FA region.

$$V_{BE}(FA) = 0.7V \quad \& \quad I_C = \beta_f I_B$$

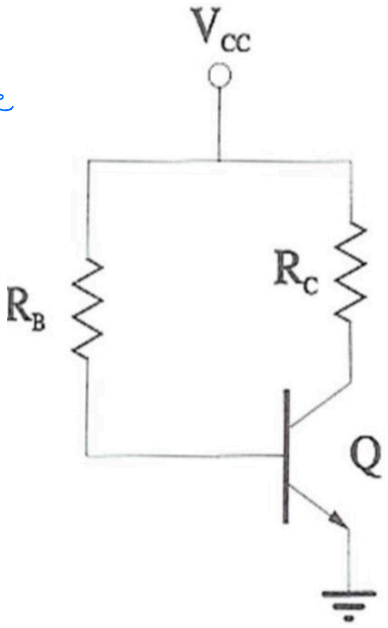
* The usual application of the self-biasing BJT is as current sink

* The desired value of V_{CE} must be selected before values for the resistors can be chosen.

$$I_B = \frac{V_{CC} - V_{BE}(FA)}{R_B}$$

$$I_C = \beta_f I_B = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\frac{R_B}{R_C} = \beta_f \frac{V_{CC} - V_{BE}(FA)}{V_{CC} - V_{CE}}$$



Self-Biasing BJT

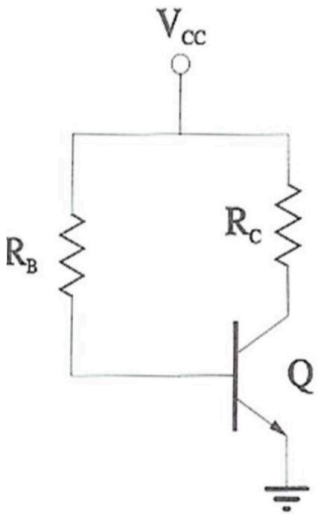
$\frac{R_B}{R_C} \approx \beta_F$ because $V_{BE} \approx V_{CE}$

* R_B should be the largest resistance since $I_B < I_C$

* The ratio R_B/R_C determines how hard the BJT is driven & thus the magnitude of stored charge in the base

Example 4.6 ***Self-Biasing BJT***

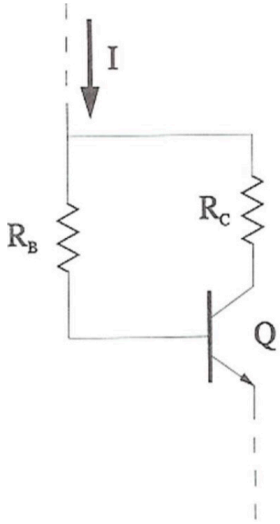
Determine the ratio R_B/R_C for a self-biasing BJT with $V_{CE} = 0.6$ V. Let $V_{CC} = 4$ V and $\beta_F = 60$.



$$\frac{R_B}{R_C} = \beta_f \frac{V_{CC} - V_{BE(FA)}}{V_{CC} - V_{CE}}$$

$$= 60 \times \frac{4 - 0.7}{4 - 0.6} = 58.2$$

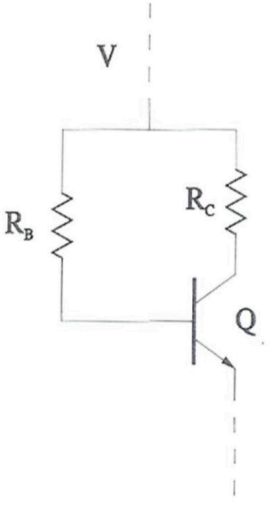
* The self-biasing BJT is exploited in BJT digital circuits for the purposes of sinking current sourcing and driving currents



Current sinking self-biasing BJT

configuration in which an incoming current is said to be sinked

configuration where the operating voltage is determined by a node voltage of another portion of the circuit.



Self-biasing BJT operating from neighboring node voltage

Power Dissipation of Bipolar Logic Circuits

*For bipolar logic circuits that have a single power supply:

$$P_{cc} = I_{cc} V_{cc}$$

I_{cc} = the current supplied by V_{cc} and it is obtained by summing all the currents leaving the supply voltage source.

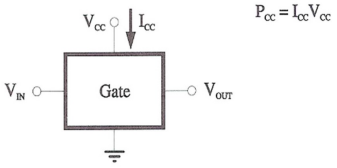


FIGURE 4.13 Power Supplied to a Logic Gate

For the bipolar logic gate of the figure to the right the current supplied by V_{cc} is

$$I_{cc} = I_{RB} + I_{RC} + I_{RCP}$$

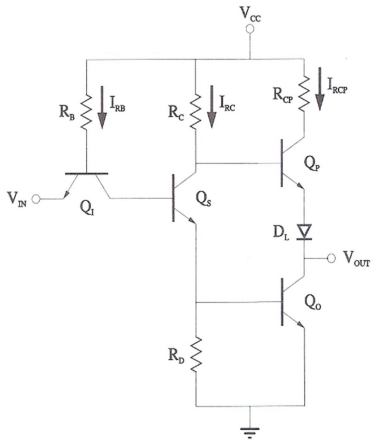


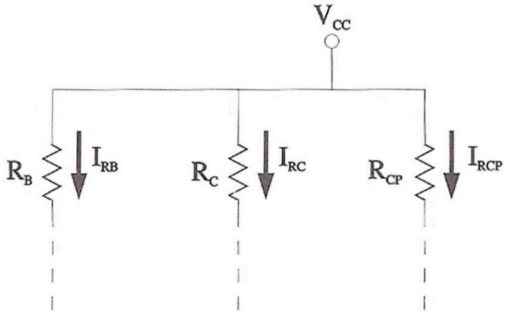
FIGURE 4.14 Current Supplied to a Bipolar Logic Gate

The average power dissipated in a logic circuit with two output is defined as:

$$P_{cc(avg)} = \left(\frac{I_{cc(OH)} + I_{cc(OL)}}{2}\right) V_{cc}$$

Example 4.7 ***Average Power Dissipation***

Figure 4.15 shows the top portion of a bipolar logic gate. The resistor currents for the output high state are $I_{RB}(OH) = 1.55$ mA, $I_{RC}(OH) = 24.7$ μA, $I_{RCP}(OH) = 1.21$ mA, and for the output low state $I_{RB}(OL) = 1.14$ mA, $I_{RC}(OL) = 4.48$ mA, and $I_{RCP}(OL) = 104$ μA. What is the average power dissipated in this gate?



$$I_{cc}(OH) = I_{RB}(OH) + I_{RC}(OH) + I_{RCP}(OH)$$
$$= 1.55m + 24.7\mu + 1.21m$$
$$= 2.78\ mA$$

$$I_{cc}(OL) = I_{RB}(OL) + I_{RC}(OL) + I_{RCP}(OL)$$
$$= 1.14m + 4.48m + 104\mu$$
$$= 5.72\ mA$$

$$P_{cc(avg)} = \left(\frac{I_{cc(OH)} + I_{cc(OL)}}{2}\right) V_{cc} = \left(\frac{2.78m + 5.72m}{2}\right) \times 5$$

$$P_{cc(avg)} = 21.3\ mW$$